

Figure 1

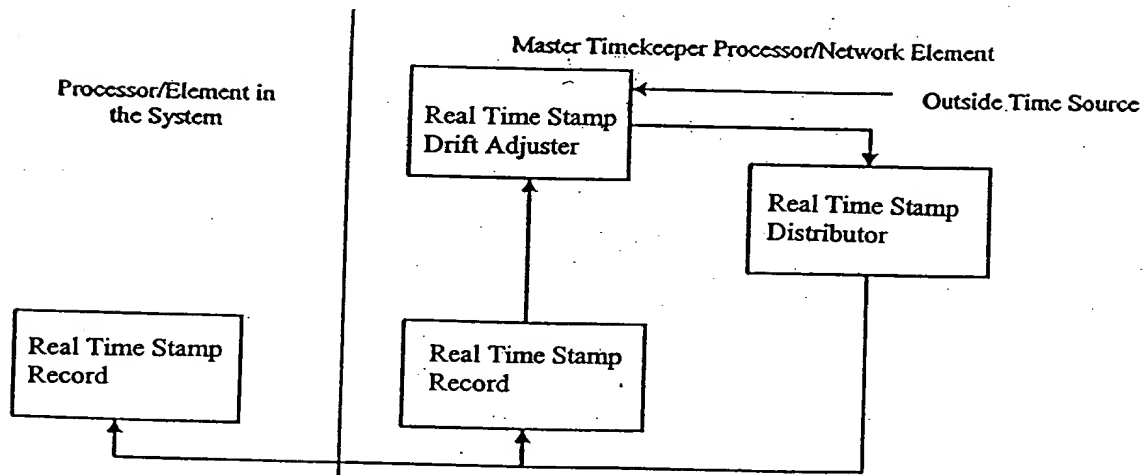


Figure 2

The diagram illustrates a distributed system architecture with the following components and connections:

- Master timekeeper 1**: Contains a **Control Circuitry** block and a **Distribution and Error Detection Circuitry** block. The Control Circuitry is connected to the Distribution and Error Detection Circuitry via a solid line. The Distribution and Error Detection Circuitry is connected to the Backplane via a dashed line. Below the Distribution and Error Detection Circuitry are multiple **Receiver Circuitry for Processor** blocks, labeled **Processor 1** and **Processor N**, connected by a vertical line.
- Master timekeeper M**: Contains a **Control Circuitry** block and a **Distribution and Error Detection Circuitry** block. The Control Circuitry is connected to the Distribution and Error Detection Circuitry via a solid line. The Distribution and Error Detection Circuitry is connected to the Backplane via a dashed line. Below the Distribution and Error Detection Circuitry are multiple **Receiver Circuitry for Processor** blocks, labeled **Processor 1** and **Processor N**, connected by a vertical line.
- Backplane**: A central vertical dashed line representing the communication bus connecting the Distribution and Error Detection Circuitry blocks of all Master timekeepers and System Elements.
- System Element 1**: Contains a **Distribution and Error Detection Circuitry** block and multiple **Receiver Circuitry for Processor** blocks, labeled **Processor 1** and **Processor N**. The Distribution and Error Detection Circuitry is connected to the Backplane via a dashed line. The Receiver Circuitry blocks are connected to the Distribution and Error Detection Circuitry via a vertical line.
- System Element N**: Contains a **Distribution and Error Detection Circuitry** block and multiple **Receiver Circuitry for Processor** blocks, labeled **Processor 1** and **Processor N**. The Distribution and Error Detection Circuitry is connected to the Backplane via a dashed line. The Receiver Circuitry blocks are connected to the Distribution and Error Detection Circuitry via a vertical line.

Vertical ellipses between Master timekeeper 1 and Master timekeeper M, and between System Element 1 and System Element N, indicate that there are multiple instances of these components in the system.

Figure 3

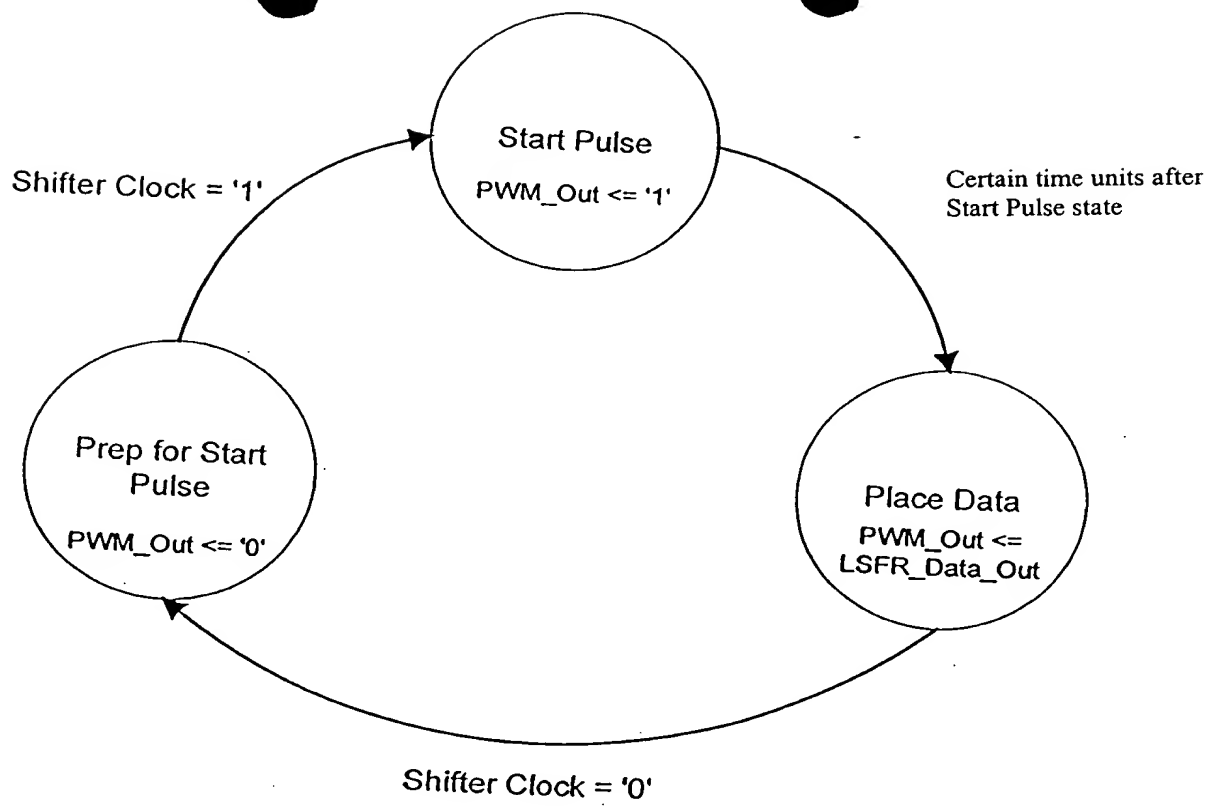


Figure 4

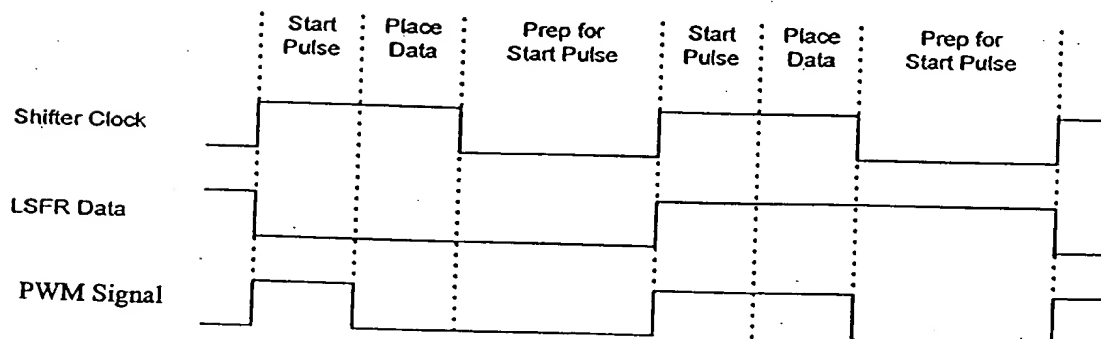


Figure 5

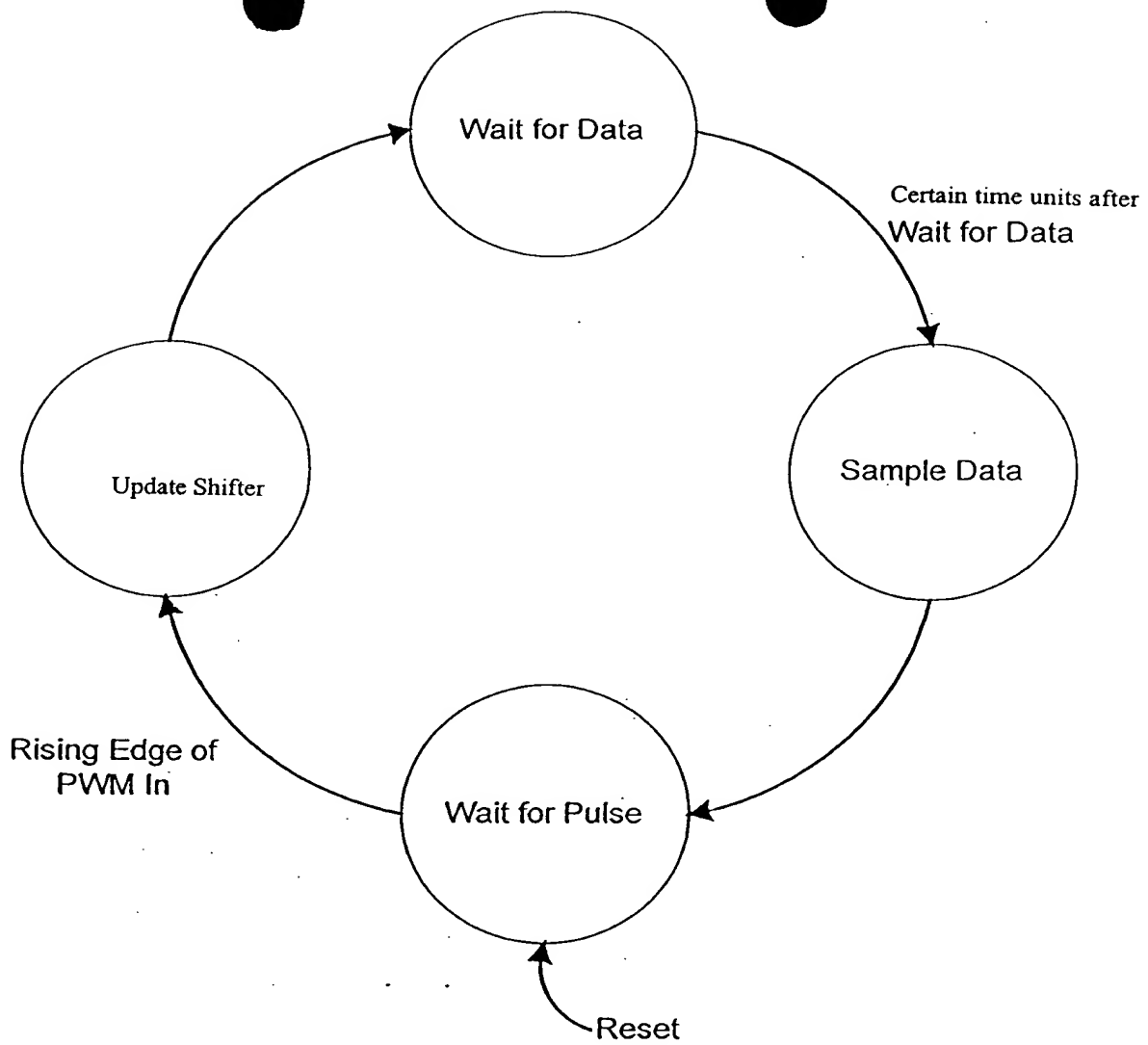


Figure 6

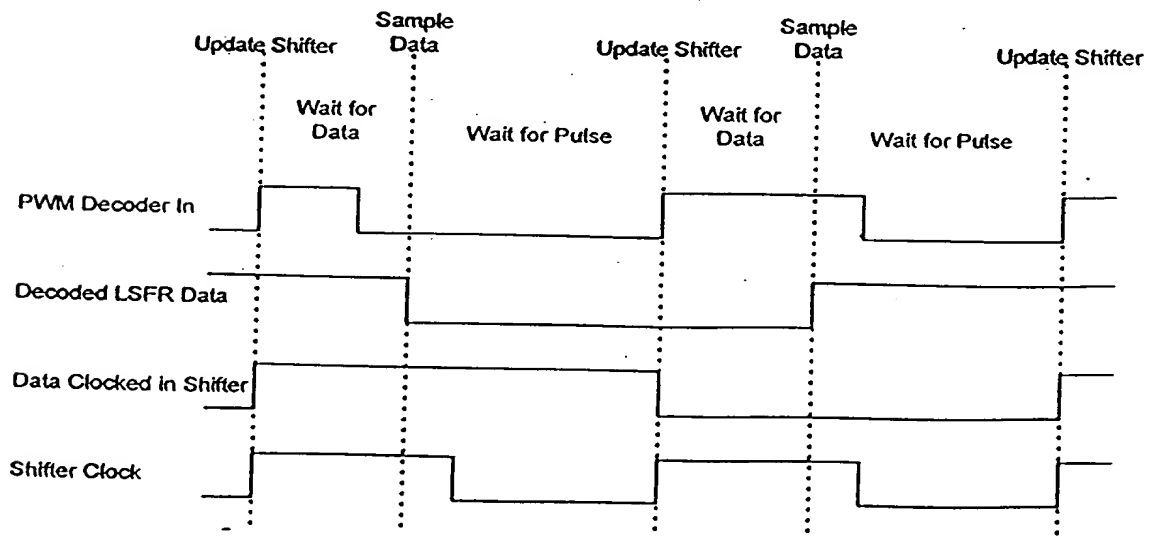


Figure 7